REMARKS

Please reconsider the application in view of the above amendments and the following remarks. Applicant thanks the Examiner for carefully considering this application. In addition, Applicant thanks the Examiner for courtesies extended during the Examiner Interview conducted on September 18, 2007.

Disposition of Claims

Claims 1, 2, 6-7, 16-18 and 37-42 are pending. Claims 3-5, 8-15 and 19-36 are cancelled by this reply without prejudice of disclaimer. New claims 37-42 are added by this reply. Claims 1, 37, and 40 are independent. The remaining claims depend, directly or indirectly, from claims 1, 37, and 40.

Claim Amendments

Claim 1 has been amended to include the subject matter of cancelled claims 4 and 5. Further, claims 6 and 7 have been amended to now depend from amended claim 1 and claim 16 has been amended for consistency with amendments made to amended claim 1. New claim 37 includes the subject matter of claim 1 and cancelled claims 8 and 9. New dependent claim 38 includes the subject matter of cancelled claim 10. New dependent claim 39 includes the subject matter of cancelled claim 11. New claim 40 includes the subject matter of claim 1 and cancelled claims 11 and 12. New dependent claim 41 includes the subject matter of cancelled claim 15. New dependent claim 42

includes the subject matter of cancelled claim 16. No new matter has been added by way of these amendments.

Rejection(s) under 35 U.S.C § 101

Claim 19-36 stand rejected under 35 U.S.C. § 101 as being directed to non-statutory subject matter. Claims 19-36 are cancelled by this reply. Accordingly, this rejection is now moot.

Rejection(s) under 35 U.S.C § 102

Claims 1-36 are rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent 7,065,633 B1 ("Yates"). Claims 3-5, 8-15 and 19-36 are cancelled by this reply. Accordingly, this rejection is now moot with respect to the cancelled claims. To the extent that this rejection may still apply to the amended claims, the rejection is respectfully traversed.

Turning to the rejection, "[a] claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). (MPEP § 2131). In addition, "the identical invention must be shown in as complete detail as the claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). Furthermore, "the elements must be arranged as required by the claim" (*See* MPEP 2131).

Applicant asserts that Yates does not anticipate each and every element of the claimed invention arranged as required by the claim. Specifically, independent claim 1, as amended, requires that:

```
wherein emulating the original instruction comprises
      emulating a pushl instruction, and
wherein emulating the pushl instruction comprises:
      obtaining a stack pointer location, wherein the
            stack pointer location corresponds to a
            location in the stack frame;
      incrementing an instruction pointer to obtain
            an incremented instruction pointer;
      loading the incremented instruction pointer in
            the stack frame at one location before
            the stack pointer location;
      loading a code segment (CS) value stored one
            location after the stack pointer location
            into the stack pointer location;
      loading an EFLAGS value stored two locations
            after the stack pointer location into one
            location after the stack pointer; and
      loading a base pointer into two locations after
            the stack pointer location.
```

The above limitations require specific data to be loaded into specific registers and specific operations to be performed on the data once it is loaded into the registers. While Yates may disclose data and registers, Yates fails to disclose the specific elements of the emulation as recited in amended independent claim 1. Accordingly, amended independent claim 1 is patentable over Yates. Dependent claims are patentable over Yates for at least the same reasons. Accordingly, withdrawal of this rejection is respectfully requested.

New Claims

New independent claim 37 recites, in part,

```
wherein emulating the original instruction comprises
      emulating an enter instruction
wherein emulating the enter instruction comprises:
      obtaining a stack pointer location, wherein the
            stack pointer location is corresponds to
            a location in the stack frame;
      incrementing an instruction pointer to obtain
            an incremented instruction pointer;
      loading the incremented instruction pointer in
            the stack frame at one location before
            the stack pointer location;
      loading a code segment (CS) value stored one
            location after the stack pointer location
            into the stack pointer location;
      loading an EFLAGS value stored two locations
            after the stack pointer location into one
            location after the stack pointer;
      loading a base pointer into two locations after
            the stack pointer location; and
      loading the base pointer into a base pointer
            register.
```

The above limitations require specific data to be loaded into specific registers and specific operations to be performed on the data once it is loaded into the registers. While Yates may disclose data and registers, Yates fails to disclose the specific elements of the emulation as recited in new independent claim 37. Accordingly, new independent claim 37 is patentable over Yates. Dependent claims are patentable over Yates for at least the same reasons.

New independent claim 40 recites, in part,

```
wherein emulating the original instruction comprises
      emulating a popl instruction,
wherein emulating the popl instruction comprises:
      obtaining a stack pointer location, wherein the
            stack pointer location corresponds to a
            location in the stack frame;
      loading a base pointer obtained from three
            locations after the stack pointer
            location into a base pointer register;
      loading an EFLAGS value stored two locations
            after the stack pointer location into
            three locations after the stack pointer
            location;
      loading a code segment (CS) value stored one
            location after the stack pointer location
            into two locations after the stack
            pointer location;
      incrementing an instruction pointer to obtain
            an incremented instruction pointer; and
      loading the incremented instruction pointer in
            the stack frame at one location before
            the stack pointer location.
```

The above limitations require specific data to be loaded into specific registers and specific operations to be performed on the data once it is loaded into the registers. While Yates may disclose data and registers, Yates fails to disclose the specific elements of the emulation as recited in new independent claim 40. Accordingly, new independent claim 40 is patentable over Yates. Dependent claims are patentable over Yates for at least the same reasons.

In view of the above, favorable action in the form of a Notice of Allowability is respectfully requested from new claims 37-42.

Conclusion

Applicant believes this reply is fully responsive to all outstanding issues and places this application in condition for allowance. If this belief is incorrect, or other issues arise, the Examiner is encouraged to contact the undersigned or his associates at the telephone number listed below. Please apply any charges not covered, or any credits, to Deposit Account 50-0591 (Reference Number 03226/342001).

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Respectfully submitted,

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